In the Claims:

Please amend claims 3, 12 and 16 without prejudice or disclaimer as follows:

1. (Original) A signal delay control circuit for use in a semiconductor memory device, the signal delay control circuit comprising:

a first reference voltage generating unit for generating a first reference voltage;

a second reference voltage generating unit for generating a second reference voltage that is lower than the first reference voltage;

a control signal generating unit for generating a clock signal to drive an operation of internal circuits; and

an impedance circuit in circuit with the first and second reference voltage generating units for generating a plurality of reference voltages to be applied to respective ones of the internal circuits, wherein each of the reference voltages is set in accordance with a distance between the control signal generating unit and the respective one of the internal circuits.

2. (Original) The signal delay control circuit of claim 1, wherein the internal circuits are one of the group comprising data output circuits, address input circuits, and sense amplifier drive circuits.

3. (Currently Amended) ~~(A)~~ The signal delay control circuit of claim 1, wherein the impedance circuits comprises; ~~(for use in a semiconductor memory device, the signal delay control circuit comprising:~~

~~a first reference voltage generating unit for generating a first reference voltage;~~

~~a second reference voltage generating unit for generating a second reference voltage that is lower than the first reference voltage;~~

~~a control signal generating unit for generating a clock signal to control input and output operations for data bits;)~~

a resistive circuit in circuit with the first and second reference voltage generating units for generating ~~(a)~~ the plurality of reference voltages; and

a plurality of data output units for outputting data bits from the semiconductor memory device in response to a respective one of the reference voltages, each of the

reference voltages corresponding to a distance between the control signal generating unit and a respective one of the data output units.

4. (Original) The signal delay control circuit of claim 3, wherein the first reference voltage generating unit comprises:

a load element connected between a power supply voltage terminal and an output terminal; and

a plurality of diode elements connected in series between the output terminal and a ground voltage terminal.

5. (Original) The signal delay control circuit of claim 3, wherein the second reference voltage generating unit comprises:

a load element connected between a power supply voltage terminal and an output terminal; and

a plurality of diode elements connected in series between the output terminal and a ground voltage terminal.

6. (Original) The signal delay control circuit of claim 5, wherein the load element is a PMOS transistor whose gate is grounded.

7. (Original) The signal delay control circuit of claim 3, wherein the resistive circuit comprises:

a plurality of resistors connected between the first and second reference voltage generating units; and

a plurality of nodes, each of the nodes being connected to a respective one of the data output units.

8. (Original) The signal delay control circuit of claim 3, wherein the respective reference voltage of each of the data output units is proportional to the distance between the control signal generating unit and the respective data output unit.

9. (Original) The signal delay control circuit of claim 3, wherein each of the data output units comprises:

a clock driver for outputting the clock signal provided from the control signal generating unit in response to the respective reference voltage;

a transmission circuit for latching and transferring a data bit in response to the clock signal provided from the clock driver; and

a data driver for outputting the data bit from the transmission circuit.

10. (Original) The signal delay control circuit of claim 9, wherein the clock driver comprises:

an inverter for converting the clock signal supplied from the control signal generating unit into an inverted clock signal; and

a switch for controlling an output of the inverted clock signal in response to the reference voltage.

11. (Original) The signal delay control circuit of claim 10, wherein the clock driver operates in accordance with a turn-on resistance of the switch in order to compensate a slope of a rising edge of the clock signal.

12. (Currently Amended) ~~(A)~~ The signal delay control circuit of claim 1, wherein the impedance circuits comprises; ~~(for use in a semiconductor memory device, the signal delay control circuit comprising:~~

~~a first reference voltage generating unit for generating a first reference voltage;~~

~~a second reference voltage generating unit for generating a second reference voltage that is lower than the first reference voltage;~~

~~a control signal generating unit for generating a clock signal to control input operations for address bits;)~~

a resistive circuit in circuit with the first and second reference voltage generating units for generating ~~(a)~~ the plurality of reference voltages; and

a plurality of address input circuits for controlling strobe operations in response to a respective one of the reference voltages, each of the reference voltages corresponding to a distance between the control signal generating unit and a respective one of the address input circuits.

13. (Original) The signal delay control circuit of claim 12, wherein each of the address input circuits receives the respective reference voltage that is inversely proportional to the distance between the control signal generating unit and the address input circuit.

14. (Original) The signal delay control circuit of claim 12, wherein each of the address input circuits comprises:

an input circuit for receiving an address bit supplied;

a delay circuit for delaying the address bit by a predetermined time in response to the respective reference voltage; and

a strobe circuit for admitting the address bit supplied from the delay circuit to an internal circuit of the semiconductor memory device in response to the clock signal.

15. (Original) The signal delay control circuit of claim 12, wherein the resistive circuit comprises:

a plurality of resistors connected between the first and second reference voltage generating units; and

a plurality of nodes, each of the nodes being connected to a respective one of the address input circuits.

16. (Currently Amended) ~~(A)~~ The signal delay control circuit of claim 1, wherein the impedance circuits comprises; ~~(for use in a semiconductor memory device, the signal delay control circuit comprising:~~

~~a first reference voltage generating unit for generating a first reference voltage;~~

~~a second reference voltage generating unit for generating a second reference voltage that is lower than the first reference voltage;~~

~~a control signal generating unit for generating a clock signal to control operations of sense amplifiers;)~~

a resistive circuit in circuit with the first and second reference voltage generating units for generating ~~(a)~~ the plurality of reference voltages; and

a plurality of sense amplifier drive circuits for controlling operations of respective ones of sense amplifiers in response to a respective one of the reference voltages, each of the reference voltages corresponding to a distance between the control signal generating unit and a respective one of the address input circuits.

17. (Original) The signal delay control circuit of claim 16, wherein each of the sense amplifiers drive circuits receives the respective reference voltage that is proportional to the distance between the control signal generating unit and the sense amplifier drive circuit.

18. (Original) The signal delay control circuit of claim 16, wherein the sense amplifier drive circuits comprises:

a sense amplifier array for receiving the clock signal supplied from the control signal generating unit; and

a sense amplifier driver for activating the sense amplifier array in response to the respective reference voltage.

19. (Original) The signal delay control circuit of claim 16, wherein the resistive circuit comprises:

a plurality of resistors connected between the first and second reference voltage generating units; and

a plurality of nodes, each of the nodes being connected to a respective one of the sense amplifier drive circuits.

20. (Original) The signal delay control circuit of claim 16, wherein the second reference voltage generating unit comprises a ground voltage terminal.